Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method comprising:

storing an instruction and a multiple bit exception status information word, the state of bits of said multiple bit exception word representing multiple different kinds of exceptions; and

issuing the instruction and at least part of the exception status information in parallel.

2. (Currently Amended) The method of Claim 1, further comprising:

detecting ~~the~~ a width of the instruction prior to said issuing the instruction and at least part of the exception status information in parallel.

3. (Currently Amended) The method of Claim 1, wherein said issuing the instruction and at least part of exception status information in parallel comprises:

sending the instruction to a decoder; and

sending the exception status information through an OR gate to exception handling logic.

4. (Original) The method of Claim 1, further comprising:

fetching at least one data block;

generating exception status information about the data block;

storing the exception status information with the data block; and

detecting at least part of an instruction within the data block.

5. (Original) The method of Claim 4, wherein generating exception status information includes generating information identifying that a particular exception condition was detected.

6. (Original) The method of Claim 4, wherein generating exception status information comprises generating information indicating that a particular exception condition was not detected.

7. (Original) The method of Claim 4, further comprising:

if only part of the instruction is in the data block, fetching another data block containing the rest of the instruction prior to issuing the instruction.

8. (Currently Amended) The method of Claim [[4]] 7, wherein said storing the exception status information ~~with the data block comprises storing the exception status information and the data block in a prefetch unit~~ represents the whole instruction in the multiple data blocks.

9. (Canceled)

10. (Currently Amended) An apparatus comprising:

a control unit ~~including~~:

which operates to fetch at least one data block,

generate exception status information about the data block,

a prefetch unit comprising at least ~~one~~ two prefetch buffers, wherein, the control unit is adapted to issue the instruction and at least part of the exception status information in parallel,

and to store the exception status information and the data block in the prefetch unit;

detect at least part of an instruction within the data block;

fetch another data block;

generate exception status information about the another data block; and

store the exception status information and the another data block in the prefetch unit.

11-12. (Canceled)

13. (Original) The apparatus of Claim 10, the control unit further comprising an instruction alignment unit coupled to the prefetch unit, the instruction alignment unit adapted to align the instruction before the instruction is issued.

14. (Original) The apparatus of Claim 10, further comprising a decoder coupled to the control unit, the control unit further including exception handling logic,

wherein issuing the instruction and at least part of the exception status information in parallel comprises:

sending the instruction to the decoder; and

sending the exception status information through an OR gate to the exception handling logic.

15. (Original) The apparatus of Claim 10, further comprising memory coupled to the control unit, wherein fetching at least one data block comprises fetching at least one data block from memory.

16. (Original) The apparatus of Claim 10, the control unit further including a memory device, and wherein the prefetch unit resides in the memory device.

17. (Currently Amended) A system comprising:

a static random access memory device; and

a processor coupled to the memory device, wherein the processor includes an execution unit and a control unit, the control unit including a prefetch unit and exception handling logic, the control unit adapted to:

fetch at least one data block;

generate exception status information about the data block, the exception status information being a multiple bit exception status information word, the state of said multiple bit exception word representing multiple different kinds of exceptions;

store the exception status information and the data block in the prefetch unit;

detect at least part of an instruction within the data block;

in parallel, issue the instruction to the execution unit and issue at least part of the exception status information to the exception handling logic.

18. (Original) The system of Claim 17, wherein the control unit is further adapted to:

fetch another data block;

generate additional exception status information about the another data block; and

store the additional exception status information and the another data block in the prefetch unit.

19. (Original) The system of Claim 17, wherein the prefetch unit includes at least two prefetch buffers.

20. (Original) The system of Claim 17, wherein issuing the instruction and at least part of exception status information in parallel comprises:

sending the instruction to the decoder; and

sending the exception status information through an OR gate to the exception handling logic.